Claims

1. A method of modifying an integrated circuit, the method including the steps of:
   - selecting a scaling factor,
   - scaling the circuit according to the scaling factor, and
   - adjusting the circuit for functionality and design rule compliance.

2. A method according to claim 1, wherein the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios.

3. A method according to claim 2, wherein the predetermined scaling ratios include the interconnect scaling ratio, the via size ratio and the electrical component geometry ratio.

4. A method according to claim 2 or claim 3, wherein the scaling factor is selected by rounding up to the next whole grid point from the largest of the predetermined scaling ratios.

5. A method according to any one of the preceding claims, wherein the step of scaling the circuit according to the scaling factor circuit includes multiplying the co-ordinates of the circuit geometry by the scaling factor.

6. A method according to any one of the preceding claims, wherein the step of adjusting the circuit for functionality and design rule compliance includes a hierarchical layer scaling process.

7. A method according to claim 6, wherein the hierarchical layer scaling process includes the step of scaling the components in a layer according to a predetermined layer scaling factor.

8. A method according to claim 7, wherein the hierarchical layer scaling process includes the step of scaling the components so as to maintain the connectivity of those components.

9. A method according to claim 7 or claim 8, wherein the hierarchical layer scaling process includes the step of identifying components that meet predetermined width criteria, and scaling only components that do not meet those criteria.

10. A method according to any one of the preceding claims, wherein the step of adjusting the circuit for functionality and design rule compliance includes a transistor edge adjustment process.

11. A method according to claim 10, wherein the transistor edge adjustment process includes the step of adjusting the width of the polysilicon layer and/or the length of the diffusion layer.

12. A method according to any one of the preceding claims, including the step of updating the contacts and vias.

13. A method according to claim 12, wherein the step of updating the contacts and vias includes removing the existing contacts and vias and replacing them with new contacts and vias.

14. A method according to any one of the preceding claims, including the step of adding and/or deleting layers.

15. A method according to any one of the preceding claims, including the step of checking the circuit using a layout verification process.

16. A method according to any one of the preceding claims, including the preliminary step of analysing and modifying the circuit data.

17. A method according to any one of the preceding claims, including the step of adding a node containing design parameters to devices in the circuit.